ABSTRACT OF THE DISCLOSURE

An SRAM memory cell includes first and second inverters (14, 16) interconnected between first and second data nodes. Each inverter is formed from complementary MOS transistors (18, 20, 18', 20') connected in series between a DC voltage supply source and a grounding circuit (22). A circuit (28, 30) programs the MOS transistors by causing an irreversible degradation of a gate oxide layer of at least some of the transistors (18, 18').